MAR.040

Grounds 1 and 2

Claim 1
Citation 1

Remarks:

In Figures 2 and 3 of Citation 1, particular reference is made to a protective element through the wiring, which is provided with a diffusion region 43 (corresponding to the 1st diffusion layer of Claim 1) connected to an external terminal, and a diffusion region 46 (corresponding to the 2nd diffusion layer of Claim 1) connected to a grounded electric potential, and a diffusion region 56 (corresponding to the 3rd diffusion layer of Claim 1) in the bottom of the diffusion region 46, wherein the diffusion region 43 is enclosed by the diffusion region 43 and the diffusion region 56.

Claim 5
Citation 1

Remarks:

In Citation 1, reference is made to the fact that the diffusion region 43 becomes a contact, the diffusion regions 46 and 56 become emitters, and the substrate becomes a base, operating as a lateral type bi-polar transistor.

Claim 6
Citation 1

Remarks:

In Citation 1, the diffusion region 43 and the diffusion region 46 are separated by an element separator 45.

Ground 2

Claims 2 and 3
Citations 1 and 2

Remarks:

Figures 1 and 8 of Citation 2 disclose technology wherein, ESD durability is improved in a protective circuit by using a parasitic bipolar transistor, forming a high density well (corresponding to the 4th diffusion layer of Claim 2) from the substrate in substrate 1, and making the impurity concentration of the surface of the well to be higher than the concentration on the inside.

Furthermore, the use of the technology disclosed in Citation 2 to increase the protection performance and improve ESD durability could be easily conceived by one skilled in the Art.

Claims 5 and 6
Citations 1 and 2

Remarks:

Reference is made to the remarks column relating to Claims 5 and 6 of Ground 1.

Claims 7 and 8
Citations 1, 2, 3 and 4

Remarks:

As explained in Citations 3 and 4, whether to form a protective circuit which uses a parasitic bipolar transistor operation in which an element separation region is interspersed between 2 diffusion layers, or to form it using an MOS transistor is nothing more than that which could be appropriately established by one skilled in the Art in accordance with the design. In addition, since, at the time of forming a protective circuit, using an MOS transistor and forming the gate electrode to be cylindrical in shape is also nothing more than a simple matter of design, and there is no exceptional difficulty recognized to the invention relating to Claims 7 and 8.

Claims 9 and 10
Citations 1, 2, 3 and 4

Remarks:

Figure 1 of Citation 4 particularly discloses technology for forming a protective circuit using only a difficult to break P channel MOS transistor as the protective element. Reference is made to the fact that at this time one P channel type MOS transistor gate electrode is connected to a signal line, and one more P channel type MOS transistor gate electrode is connected to an electric power source electric potential.

Furthermore, in Citation 1, the use of the technology disclosed in Citation 4 to increase the durability of the protective element itself is something which could be easily conceived by one skilled in the Art.

Claims 11 and 12
Citations 1, 2 and 3

Remarks:

Whether to make the conductive type parasitic bipolar transistor which forms a protective circuit to be NPN or to be PNP is a matter of design, appropriately determined by one skilled in the Art corresponding to a desired circuit, and there is no recognized exceptional difficulty.

Reference Citation List

1. Japanese Laid Open Patent Publication Hei 03-184369
2. Japanese Laid Open Patent Publication Hei 08-051188
3. Japanese Laid Open Patent Publication Hei 09-036357
4. Japanese Laid Open Patent Publication Hei 10-340996